IESE HOME : SEARCH IEEE : SHOP : WEB ACCOUNT ! CONTACT IEEE



Membership Publica	stions/Services Standards Conferences Careers/Jobs
Jaja	
<u> Help FAQ Terms IEE</u>	E Peer Review Quick Links ** Se
Mescario la IEEE Aglanti	·
O- Home O- What Can I Access? O- Log-out	Your search matched 4 of 1131693 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order.
Tables of Cortains	Refine This Search:
O- Journals & Magazines	You may refine your search by editing the current search expression or enterinew one in the text box. (area optimal) <and> (technology mapping) Search</and>
O- Conference Proceedings	Check to search within this result set
O- Standards	Results Key:
Search	JNL = Journal or Magazine CNF = Conference STD = Standard
O- By Author O- Basic O- Advanced O- CrossRef Lighter Statists O- Join IEEE	1 Technology mapping for simultaneous gate and interconnect optimisation Lu, A.; Stenz, G.; Eisenmann, H.; Johannes, F.M.; Computers and Digital Techniques, IEE Proceedings-, Volume: 146, Issue: 1, Jan. 1999 Pages:21 - 31
O- Establish IEEE Web Account	[Abstract] [PDF Full-Text (1124 KB)] IEE JNL
O- Access the IEEE Member Digital Library	2 A technology mapper for Xilinx FPGAs Chikodikar, M.Y.; Laddha, S.; Sirasao, A.; VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997 Pages: 57 - 61
O- Access the IEEE Enterprise File Cubinet	[Abstract] [PDF Full-Text (380 KB)] IEEE CNF
Print Format	3 A comparing study of technology mapping for FPGA Martin, HG.; Rosenstiel, W.; Design, Automation and Test in Europe, 1998., Proceedings, 23-26 Feb. 1998 Pages: 939 - 940
	[Abstract] [PDF Full-Text (16 KB)] IEEE CNF

4 Non-disjoint decomposition of Boolean functions and its application FPGA-oriented technology mapping

Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.; EUROMICRO 97. 'New Frontiers of Information Technology'., Proceedings of th 23rd EUROMICRO Conference, 1-4 Sept. 1997 Pages: 24 - 30 ieee home : Search ieee : Shop : Web account : Contact ieee



Membership Publica	Welcome United States Patent and Trademark Office
Help FAQ Terms IEE	E Peer Review Quick Links * Se
Melconic to IEEE Xolore	
O- Home O- What Can I Access? O- Log-out	Your search matched 4 of 1131693 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order.
Febres of Contents O- Journals	Refine This Search: You may refine your search by editing the current search expression or enterinew one in the text box.
& Magazines — Conference Proceedings	(area optimal) <and> (technology mapping) Check to search within this result set</and>
O- Standards States	Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard
O- By Author O- Basic O- Advanced O- GrossRef	1 Technology mapping for simultaneous gate and interconnect optimisation Lu, A.; Stenz, G.; Eisenmann, H.; Johannes, F.M.; Computers and Digital Techniques, IEE Proceedings-, Volume: 146, Issue: 1, Jan. 1999 Pages:21 - 31
O- Join IEEE O- Establish IEEE	[Abstract] [PDF Full-Text (1124 KB)] IEE JNL
Web Account O- Access the IEEE Member Digital Library	2 A technology mapper for Xilinx FPGAs Chikodikar, M.Y.; Laddha, S.; Sirasao, A.; VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997 Pages:57 - 61
Or Access the IEEE Enterprise File Cabinet	[Abstract] [PDF Full-Text (380 KB)] IEEE CNF
E Print Format	3 A comparing study of technology mapping for FPGA Martin, HG.; Rosenstiel, W.; Design, Automation and Test in Europe, 1998., Proceedings, 23-26 Feb. 1998 Pages:939 - 940
	[Abstract] [PDF Full-Text (16 KB)] IEEE CNF
	4 Non-disjoint decomposition of Boolean functions and its application FPGA-oriented technology mapping Rawski, M.; Jozwiak, L.; Nowicka, M.; Luba, T.;

23rd EUROMICRO Conference, 1-4 Sept. 1997

Pages:24 - 30

EUROMICRO 97. 'New Frontiers of Information Technology'., Proceedings of th

HESE HOME I SEARCH HEEF : SHOP I WEB ACCOUNT I CONTACT HEEF



lá a m	bership Public	rations/Services Standards Conferences Careers/Jobs
		Welcome United States Patent and Trademark Office
<u>Help</u>	FAQ Terms 1E	EE Peer Review Quick Links * S
	me to IEEE <i>Xplore</i> :	
Ö	Home What Can I Access? Log-out	Your search matched 4 of 1131693 documents. A maximum of 500 results are displayed, 15 to a page, sorted by Relevance Descending order.
	s of Contents	Refine This Search:
200000000000000000000000000000000000000	Journals & Magazines	You may refine your search by editing the current search expression or enter new one in the text box. (depth optimal) <and> (technology mapping) Search</and>
0	Conference	(depth optimal) <and> (technology mapping) Check to search within this result set</and>
()-	Proceedings Standards	
Spane		Results Key: JNL = Journal or Magazine CNF = Conference STD = Standard

	By Author	Church and make decomposition for double outlined to be also as a second
***	Basic	1 Structural gate decomposition for depth-optimal technology mapping LUT-based FPGA design
	Advanced	Cong, J.; Yean-Yow Hwang;
	CrossRef	Design Automation Conference Proceedings 1996, 33rd, 3-7 June 1996
		Pages:726 - 729
Ò	Join IEEE	[Abstract] [PDF Full-Text (388 KB)] IEEE CNF
\	Establish IEEE Web Account	2 On area/depth trade-off in LUT-based FPGA technology mapping
0	Access the	Cong, J.; Yuzheng Ding;
	IEEE Member Digital Library	Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume 2 , Issue: 2 , June 1994
	22 133 1 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Pages:137 - 148
0	Access the IEEE Enterprise	[Abstract] [PDF Full-Text (1072 KB)] IEEE JNL
	File Cabinet	3 DAOmap: a depth-optimal area optimization mapping algorithm for designs
⊞ . ₽	rint Format	Chen, D.; Cong, J.; Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Confere on , 7-11 Nov. 2004 Pages:752 - 759
		[Abstract] [PDF Full-Text (908 KB)] IEEE CNF

4 Hermes: LUT FPGA technology mapping algorithm for area minimiza with optimum depth

Teslenko, M.; Dubrova, E.;

Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conferer on , 7-11 Nov. 2004